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FINAL REPORT – PHASE I

FIELD EMITTER ARRAY RF AMPLIFIER DEVELOPMENT PROJECT

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MCNC ELECTRONIC TECHNOLOGIES DIVISION

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Field Emitter Array RF Amplifier Development Project

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This document presents the results of Phase I of the Field Emitter Array RF Amplifier Development Project. The primary goal of the Phase I performance period was the development of field emission cathodes with the following characteristics: 5 mA total emission current, 5 A/cm^2 current density, operation at an applied voltage of less than 250 V, greater than 1 hour lifetime, and emission current modulation at 1 GHz or greater. The basic fabrication process for silicon field emitter arrays was defined during the first 18 months of the contract performance period. During the final 12 months of the contract, the process was refined using statistical process control, with the goal of maximizing electrical yield on large arrays. The resulting devices met each of the program performance criteria. Arrays of up to 232,630 emitters, the largest field emitter arrays in any material to date, were successfully fabricated and electrically tested. The emission currents measured from these devices were the highest reported in the literature for silicon field emitter arrays. Techniques for further enhancing performance through the deposition of low work function and metal coatings were developed. Recommended directions for further research were defined for implementation under ARPA leadership.

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1. SUMMARY

This document presents the results of Phase I of the Field Emitter Array RF Amplifier Development Project. The primary goal of the Phase I performance period was the development of field emission cathodes with the following characteristics: 5 mA total emission current, 5 A/ cm^2 current density, operation at an applied voltage of less than 250 V, greater than 1 hour lifetime, and emission current modulation at 1 GHz or greater. The basic fabrication process for silicon field emitter arrays was defined during the first 18 months of the contract performance period. During the final 12 months of the contract, the process was refined using statistical process control, with the goal of maximizing electrical yield on large arrays. The resulting devices met each of the program goals. Arrays of up to 232,630 emitters, the largest field emitter arrays in any material to date, were successfully fabricated and electrically tested. The emission currents measured from these devices were the highest reported in the literature for silicon field emitter arrays. Techniques for further enhancing performance through the deposition of low work function and metal coatings were developed. Recommended directions for further research were defined for implementation under ARPA leadership.

1.1 Milestone Performance. Performance on milestones and deliverables are given for the basic contract in Table 1 and the Option 1 performance period in Table 2 and Table 3. A GANTT chart is given for the Option 1 contract tasks as Figure 1. No such schedule was prepared during the basic contract performance period.

1.2 Fiscal Performance. Fiscal data is given for the basic contract period in Figure 2. Total expenditures on the contract during the period from 09/09/91 through 01/15/93 were $1,216,927 relative to a contract amount of $1,178,466. Preliminary fiscal data for Option 1 of the contract based on financial data, contract commitments, and estimated processing costs through 05/15/94 is shown in Figure 3. From this preliminary data, total expenditures on the contract during the period from 04/16/93 through 05/15/94 were $461,831 relative to a follow-on contract amount of $454,965. Expenditures over the contract amounts were covered with internal funds. Complete financial information will follow in the final report from the MCNC contracts office.

Table 1. Milestone and deliverable performance during basic contract period.

Task	Completion Date	
Milestones	Original	**Complete** Expected
Complete first diodes of each of the three device types: Horizontal, vertical, and trench. Deliver samples to NRL, NCSU, and Litton. (MCNC)	11/91	**11/91**
Prepare first pass device models and potential circuit models based on initial device IV data. (Duke, MCNC, and UNC-CH)	3/92	**11/92**
Down select RF FEA designs based on device performance predictions	3/92	**12/91**
Complete first generation of field emission IV curves for each of the device types fabricated along with initial electron trajectory data and electron time of flight data. (NCSU and MCNC)	3/92	**3/92**
Design and order vacuum sealing and test system (MCNC)	11/91	**12/91**
Modify Litton trajectory modeling programs for field emission. Initial macroscale high vacuum tube encapsulation of field emission cathodes. (Litton)	3/92	**11/91**
Complete second set of field emission diode device runs with column FEAs (MCNC)	3/92	**3/92**
Complete third series of gated column emitters with modifications for very low electric fields over gate emitter isolations to reduce gate leakage	-	**5/92**
Complete new mask set for half micron field emission devices. (MCNC)	5/92	**3/92**
Install vacuum sealing and test system (MCNC) (Temporary vacuum test system in SEM chamber 3/92)	3/92	**10/92**
Complete initial electron trajectory modeling and initial testing of macroscale tubes containing microstructural gated FEC diodes. (Litton)	7/92	**10/92**
Complete fabrication of first microencapsulated FEC transistors. (MCNC)	9/92	**5/92**
Generate first pass transistor data from microencapsulated FE transistors. (MCNC, Duke, and Litton)	9/92	**9/92**
Demonstrate microstructural FEA diode/open triode devices meeting device IV and g_m/C program requirements.	9/92	**1/94**
Determine priorities of future device development. Determine the primary amplifier design methodology from the three amplifier design approaches. (MCNC)	9/92	**3/93**
Complete design for first integrated FEC based RF amplifier and FEC tube RF amplifier based on device characterizations. (MCNC, Duke, and Litton)	3/93	3/93 **POSTPONED**
Complete second level models for FEC emission from surfaces treated in various manners. (UNC-CH)	3/93	3/93 **POSTPONED**
Complete testing of FEC electron trajectories, electron trajectory model verification. (NCSU, Litton)	3/93	3/93 **POSTPONED**
Determine packaging and cooling requirements for the prototype RF amplifier. (MCNC and Litton)	3/93	3/93 **POSTPONED**

Table 2. Milestone performance during Option 1 contract period.

Task	Completion Date	
Milestones	Original	**Complete Expected**
Complete design and fabrication of new reticle set. Complete lot origination process for two runs of 2 μm column emitter arrays. (MCNC)	5/93	**5/93**
Complete first run of field emitter arrays (2 μm column). Complete lot origination process for two runs of 4 μm column field emitter arrays. (MCNC)	7/93	**8/93**
Complete acquisition and installation of whole wafer DC test and RF measurement equipment. Begin in-house device DC characteristics and reliability testing program. (MCNC and Duke)	7/93	**11/93**
Begin low work function and metal coating development (MCNC)	7/93	**6/93**
Complete second run of field emitter arrays (2 μm column). Deliver devices to Litton subprogram for packaging and RF testing. (MCNC)	9/93	**10/93**
Begin in-house device RF testing program. (MCNC)	8/93	**8/93**
Complete third run of field emitter arrays (4 μm column). Complete lot origination process for two runs of 4 or 6 μm column field emitter arrays. (MCNC)	10/93	**12/93**
Complete packaging, begin RF testing of field emitter amplifier modules. (Litton)	9/93	**10/93**
Complete fourth run of field emitter arrays (4 μm column). (MCNC)	10/93	**3/94**
Complete RF testing of field emitter amplifier modules. (Litton)	10/93	**12/93**
Complete fifth run of field emitter arrays (6 μm column). (MCNC)	1/94	**5/94**
Complete sixth run of field emitter arrays (6 μm column). (MCNC)	2/94	**5/94**
Complete all contract activities. Deliver devices, data, and other related material to ARPA. Complete and deliver final report according to contract stipulations. (MCNC)	4/94	**5/94**

Table 3. Deliverables performance during Option 1 contract period.

Task	Completion Date	
Deliverables	Original	**Complete** Expected
Plots of new mask design set available for inspection by ARPA personnel if desired.	5/93	**5/93**
Sample devices from the first run of field emitter arrays (2 μm column) with SEM inspection data.	7/93	**8/93**
First quarterly R&D status/technical report.	8/93	**8/93**
Sample devices from the second run of field emitter arrays (2 μm column) with SEM inspection data. Performance data from first run.	8/93	**12/93**
Sample devices from the third run of field emitter arrays (4 μm column) with SEM inspection data. Performance data from second run	9/93	**2/94**
Sample devices from the fourth run of field emitter arrays (4 μm column) with SEM inspection data. Performance data from third run	10/93	**3/94**
RF amplifier module performance data from Litton subcontract.	10/93	**12/93**
Second quarterly R&D status/technical report.	11/93	**11/93**
Sample devices from the fifth run of field emitter arrays (4 or 6 μm column) with SEM inspection data Performance data from fourth run	1/94	**5/94**
Sample devices from the sixth run of field emitter arrays (4 or 6 μm column) with SEM inspection data Performance data from fifth run	2/94	**5/94**
Third quarterly R&D status/technical report.	2/94	**2/94**
Low work function and metal coating development results Performance data from sixth run Reliability test data for all devices Final Technical Report - Option 1	4/94	**5/94**

1.3 Certification of Labor Hours Expended. The total number of hours expended under the category of direct labor during the basic contract performance period was 6.236 During the Option 1 performance period, 2.868 hours of direct labor were expended, for a total of 9104 for the entire contract. MCNC reports labor on contracts under the direct labor category only

2. TECHNICAL RESULTS

2.1 Electrical testing and high-frequency measurements. Procedures for DC testing of field emitters are well documented in the literature, and are similar between research programs. The primary differences are in the anode material and configuration, the vacuum level during testing, and the duty cycle of the voltage

applied to the gate electrode. At MCNC, testing has been performed under a variety of conditions. The development of the testing procedure and system is documented in the technical reports delivered during the contract performance period (Appendix A). The current procedure and equipment, along with test results, are detailed in a published paper [23]. Statistics from the DC testing program are shown in Table 4. Important findings are summarized in the following sections.

Table 4. Electrical yield data for devices fabricated and tested by the MCNC field emitter program, covering the period from 07/31/93 to 01/26/94.

Number of Tips in Array	Total Tested	Working	No Emission	Shorted Gate
1	27	7	20	0
100	3	2	0	1
1,197	90	54	25	11
3,255	73	31	19	23
6,648	10	8	2	0
7,347	10	3	0	7
16,092	7	0	0	7
18,309	18	3	2	13
44,460	11	5	2	4
232,630	4	1	1	2
Total	**253**	**114**	**71**	**68**
Percent		45	28	27

2.1.1 Vacuum Requirements. Although most researchers perform field emission measurements at ultra-high vacuum (UHV), product applications will require field emitter arrays to operate at ambient pressures more in the 10^{-6} torr range. Standard test procedure at MCNC dictates that the chamber reach the mid 10^{-8} torr before testing begins. The chamber walls are heated to 100 °C during evacuation, and the chamber is purged with dry nitrogen after the initial pumpdown. Following this procedure, test pressure can be reached overnight.

During testing, the anode generates heat. This heat is transmitted to the device under test directly by radiation and indirectly by conduction through the test fixture. At a certain point, the anode and device begin to outgas, and the chamber pressure rises. Device operation can continue at a fairly high level as long as the pressure remains in the 10^{-7} torr range. Once the pressure reaches the 10^{-6} torr range, however, device operation ends catastrophically. This may be due either to

destruction of the emission sites by ion bombardment, or by arcing between the anode and cathode or gate electrode and cathode.

2.1.2 Packaging. One unanticipated aspect of electrical testing at MCNC was the importance of the test vehicle in the performance of the field emitter device. Not only must the test vehicle provide a good mechanical platform for the device and anode, but reliable electrical connections as well. The package must also be able to withstand and dissipate the thermal energy generated at the anode at higher emission currents. Currently, a 24-pin ceramic dual in-line package (DIP) is the vehicle of choice for DC testing. The devices are mounted in the DIP using either conductive epoxy or solder paste, and connections are made to the gate electrodes with wirebonds.

2.1.3 Anode Material. A variety of anode materials were used during Phase I of the project. Initially, metal anodes fabricated from flat copper or brass were used on the assumption that the only requirement on the anode material was that it be conductive. Later, it became clear that anode material was being evaporated, even at low emission currents, and re-depositing on the arrays under test, short-circuiting the gate electrode to the cathode. An anode was constructed using tungsten wire that performed adequately. Some experiments were done using nickel anodes removed from vacuum tubes, but the performance of these anodes was not noticeably better.

Finally, graphite was chosen for the anode material. In addition to a higher melting point than most metals, it has the added advantage of low secondary and backscattered electron generation. Graphite anodes have been used for both DC and high frequency testing with consistently superior performance.

2.1.5 RF Test Requirements. To test field emitters at high frequency, both a DC bias and high frequency signal must be applied to the device. The DC bias circuitry required is essentially the same as the low frequency test equipment. To add high frequency capability, constant impedance (usually 50 Ω) must be maintained from the test equipment, through the walls of the vacuum chamber and the test vehicle, to the device under test. Further, the high frequency signal must be isolated from the bias supply. The RF test system was designed using SMA connectors and RG-188 cable with Teflon insulation for high temperature and high vacuum compatibility. A high frequency compatible ceramic package with gold metalization and stripline leads was chosen (Kyocera America, Inc. part number SD570-A700). Details of the RF test equipment configuration and test procedure are given in the technical reports delivered during the contract performance period (Appendix A). The best RF test results are summarized in the third special technical report. DC data taken during the

test yielded the current versus voltage curve shown in Figure 4. The corresponding output signal is shown in Figure 5.

2.2 Device processing. The current process flow for the fabrication of silicon field emission devices is given in detail in [4]. There have been numerous modifications to the basic process flow developed during the first 18 months of the contract in order to achieve the desired structures. Three basic structures have been fabricated during the Option 1 performance period: the two micron column, the four micron column and the six micron column. The column height dictates the changes in the original process flow; as the column height increases, the process becomes more complicated. Normal process variations, as well as the deviations in the devices themselves created major challenges in the fabrication of these arrays.

The first task required to fabricate the various field emitter devices was to design a reticle set that would supply the program with devices capable of fulfilling all of the contract performance requirements. The field emitter reticle sets used during the basic contract performance period were reviewed and a close examination of the design goals was made. Using this data, a new reticle set was designed. Some of the innovative design changes were: hexagonal packing of the emitter tips and various tip pitches for the optimum current density, device dimensions to simplify current density calculations, large arrays with a maximum of emitter tips to achieve high currents, the addition of high frequency bonding pads, and a project chip for the testing of single tips and small arrays of tips at several tip pitches. The resulting design is described in detail in the Quarterly R&D Status/Technical Report #7 (4/16/93 – 7/15/93).

2.2.1 Fabrication of the 2 μm Devices. In order to create the best possible devices, the entire fabrication process flow was subjected to a detailed review that included MCNC personnel outside of the field emitter program. Each process step was examined to reveal any critical variations. The first strategic process change occurred regarding the formation of the emitter tip. Understanding each of the processing steps and their relationship to the entire process was examined through the application of statistical process integration. The use of process integration allowed the identification and improvement of problem areas in the fabrication of the field emitter devices. Computer models were used to determine the optimum field emitter structure. The combination of the modeling information and the process integration data lead to the fabrication of the first functional 2 μm column field emitters. There were several key processes that required substantial attention.

The radius of curvature of the field emitter tips is one of the most important geometric parameters of the device. There are three major processing steps that effect

this parameter: the uniformity of the initial photolithography, the oxidation sharpening of the silicon emitter tip, and the etch step that defines the tip itself. Each of these processes were examined to determine the optimum parameters for the production of uniformly sharp emitter tips.

The next parameter investigated was the tip placement in the gate metal. The models indicated that the best location for the tip is to be centered both horizontally and vertically within the gate metal opening. The basic self-aligning process automatically positions the tip properly in the horizontal direction. The optimum vertical position of the gate metal is then calculated based on the combined height of the emitter tip and column. The proper amount of evaporated oxide is deposited so that the tip is centered in the gate metal after its evaporation.

Gate metal thickness was another processing issue. The gate metal thickness was dependent on the cap removal process. Using the self-aligning process, the "balloon" formed by the evaporated oxide on the cap protects the emitter tip and column from the gate metal. As the gate metal increases in thickness, the cap removal becomes more difficult. After evaluating metal layers of varying thickness, 5000 Å was selected as optimum for processing.

The cap removal process was also investigated. The ideal process allowed the caps to be removed using a chemical oxide etch alone. This was not the case with previous runs. Additional mechanical force was needed to remove the caps for 100% cap removal yield. The combination of these steps led to high cap removal yields at the end of the process. These high yields make choosing devices for electrical testing significantly easier.

There were two other process modifications that were implemented to increase the electrical performance. The first was the formation of the emitter tips using an isotropic reactive ion etch. The second was the addition of a backside metalization on the devices to allow a high vacuum compatible die attach to be used. Both of these modifications were successful and added to the success of the first 2 μm column runs.

The electrical results from the first 2 μm column runs have yielded the highest per tip currents reported in the literature to date for silicon-based devices. The optimized process also produced the largest array (232,630 emitters) reported in the literature for field emitters made from any material.

2.2.2 Fabrication of the 4 μm Column Devices. The fabrication of the 4 μm column devices follows the same process flow as the 2 μm column devices with some modifications. The 4 μm column device requires additional etch masking materials for the taller column and thicker SiO_2 insulator material between the

columns. Although these changes seem minor, they greatly complicate the fabrication process.

As the thickness of the masking materials for the formation of the column increases, various other processing parameters are affected. As detailed in [4], precise lithography is critical to the generation of uniform tips. Thicker masking films introduce variation into the photolithography. However, using the process integration techniques described above, the variation was minimized to yield the best results.

The addition of the taller column also complicates the insulator backfill process. In order to properly fill the insulator between the columns, a process was developed using evaporated oxide. This process is a combination of evaporation of SiO_2, etchback on the columns, and another evaporation to complete the process. The development of this backfill process and implementation into a standard process was completed.

The overall sharpness of the emitter tips was enhanced on the 4 μm column structures by refining the oxidation sharpening process. The resulting devices were high produced excellent DC performance. In addition, the reduction in input capacitance due to the increase in cathode to gate electrode spacing allowed these devices to produce anode current modulation at 1 GHz.

2.2.3 Fabrication of the 6 μm Devices. The 6 μm column devices presented the greatest fabrication challenge. A gated field emission device with this size column had not yet been successfully fabricated. The 6 μm column process follows the same general process flow as the previous devices, however, the additional masking material required for formation of the tall column structure complicated the process immensely.

The process variation is greatly increased as the total masking material increases. This variation can be seen primarily in the reactive ion etch (RIE) process for that material. There is a ten percent process variation in the RIE process that is related to the equipment itself. The longer the required etch time, the more this variation affects the process. This deviation is then translated into variation at the tip formation stage. This was one of the most significant problems associated with the 6 μm column devices. Through the use of a laser endpoint detection system and careful control of the etch time, the effects of the RIE nonuniformities were reduced.

The insulator backfill process was causing some problems associated with the control of the gate aperture diameter. An anomaly of the evaporation process was leaving a "collar" on the sides of the columns that was causing the gate opening diameter to be increased significantly. It was found that the formation of this collar was related to the anneal of the evaporated oxide for densification. The solution to the

problem was to remove the evaporated oxide from the columns prior to the anneal process.

The use of standard silicon processing technology has allowed the fabrication of high yield, low capacitance field emission devices. The transfer of this process to high volume manufacturing facilities is possible.

2.2.4 Encapsulated Devices. Three lots were run to fabricate a microencapsulated device using "thin film" techniques; that is, to do the encapsulation using deposition of metal and oxide films, as opposed to physically placing an encapsulating structure, such as a metal or silicon plate, on the emitter structure. These lots were called feas.encap1, feas.encap2, and feas.encap3. This structure was successfully fabricated, and preliminary testing was done, as reported in [29].

Further analysis of the test data has raised some questions as to whether these devices produced field emission. The devices require very strong fields across very thin dielectric material and are therefore susceptible to Frenkel-Poole conduction current through the dielectric film [12]. An I-V curve of Frenkel-Poole current is superficially similar to an I-V curve of field emission current according to the Fowler-Nordheim relation, and makes determination of actual field emission current difficult. And while Frenkel-Poole current is different from Fowler-Nordheim current in that it is bi-directional and temperature dependent, our test set up did not allow for temperature changes of the device under test. Bi-directional tests were performed, and in some cases there was more current in the forward direction than in the reverse. While this might indicate field emission, an analysis of the test set up, particularly the various interfaces among metal, silicon, and thin oxides that the current path must cross, makes it difficult to determine with a high level of confidence just what is causing the diode-like effect.

A further problem with this mode of encapsulation is that encapsulation of large arrays with the current reticle set requires too much undercut of the anode structure. To encapsulate large arrays successfully would require redesign of the current reticle set. It now appears a more productive approach for encapsulation of these devices would be the large-scale or macroscopic approach in which metal plates or metallized wafers would be bonded to the wafer containing the active devices under a high-quality vacuum.

2.2.5 Low-Capacitance Gate Structures. In order for field emitter triodes to be practical high-frequency devices and provide gain at frequencies of 1 GHz or higher, the gate capacitance must be minimized. The primary strategy for that in this project has been to make the emitters tall column structures in order to increase the distance between the conductive substrate and the gate metal, and thereby reduce

parallel-plate capacitance. There are, however, other approaches in addition to this, and some experiments were done to explore these approaches. A fourth reticle was designed and fabricated which allowed experiments on two methods.

Fabrication of tall wedges and columns through crystallographic etching was one approach. The etching of the silicon columns in our current devices is not perfectly anisotropic, and produces structures that are tapered rather than perfectly cylindrical. Another method of creating tall structures by utilizing the crystallographic etching of silicon wafers with a <110> orientation was examined. This type of anisotropic etching is well known, but is usually thought of in the context of etching holes in silicon, rather than creating tall free standing structures.

Due to the nature of this etch process, it is easier to produce long wedge type structures that column type structures, although both were included in this fourth reticle design. As can be seen in Figure 6, free standing structures are produced. It may be that the corners are sharp enough to produce emission with a proper gate structure. Use of these as wedge type emitters would also be attractive, since a sharp wedge would presumably have more emission area that a series of point type emitters for a given device area. This would improve transconductance, which would in turn improve gain at high frequencies.

Another approach to low capacitance structures is the reduction of gate metal area and reduction of dielectric constant of the insulating layer between the cathode and gate electrode. Most reported fabrication techniques for field emitter arrays blanket the area between the field emitter tips with metal. Most of this metal is unnecessary, and yet increases parallel-plate capacitance, which is a function of the area of the metal.

A second related approach is to reduce the dielectric constant of the volume between the substrate and gate metal. In our devices, the dielectric is SiO_2, which has a relative dielectric constant of 3.9. If this were all vacuum, the relative dielectric constant would be 1, and would thereby reduce the capacitance almost fourfold.

Such a structure has been suggested in the literature [21]. Using our devices with 10 μm micron pitch in a closely packed hex array, a low capacitance gate structure was fabricated using two of the above-mentioned approaches. One approach simply reduced the area of the gate electrode metal by allowing the gate metal to be deposited as circles around the emitter tip, with connecting lines from circle to circle, as shown in Figure 7. This reduces the metal area over the active region by about 50%. A second approach was to deposit the gate metal in straight lines, and then following an anisotropic reactive ion etch of the dielectric oxide in the areas between the metal lines, the dielectric was undercut under the metal lines with a wet

isotropic etch, leaving only small pillars of oxide between the emitter tips to support the gate metal, as shown in Figure 8. This approach combined the reduction of metal area with the reduction in the high dielectric content insulator.

Both approaches appear feasible. There are some fabrication problems to be dealt with further, particularly in using the self-aligning gate approach, but testable devices have been completed.

There are two concerns that can only be resolved by electrical testing of these devices. The first concern is whether the devices in which the gate metal is supported by the oxide pillars can withstand the strong electrostatic forces that tend to pull the gate metal towards the substrate. A second concern is whether the narrow lines around the edges of the gate openings can conduct the captured emission current without melting down. These are issues that need to be resolved through testing.

Our strategy of tall individual silicon columns has produced devices that meet the basic requirements of the current contract. It does appear that if there were further interest in fabricating devices for high-frequency applications there are additional approaches that offer a high probability of significant reductions in gate capacitance.

2.3 Development of Deposition Techniques for Low Work Function Coatings. According to the Fowler-Nordheim equation, decreasing the work function value at an electron emission site dramatically increases the emission current and transconductance for a given gate voltage. Refractory borides, nitrides and carbides of rare-earth and transition metals are known to exhibit low work function values, along with high melting points, low sputtering yield, resistance to corrosion and metallic conductivity. All of these features make them good candidates for use as emitter materials, and, in fact, some of the compounds, primarily LaB_6, have found applications as materials for thermionic cathodes and cold (field emission) electron sources in scanning electron microscopes.

Table 5 shows reported work function values, melting points, and resistivities of three of these low work function materials. During the Phase I Option 1 contract period we have developed in-house deposition techniques for all three of these materials, and extensively characterized blanket thin films formed by the developed techniques.

2.3.1 LaB_6 and ZrC Films. These films have been deposited via an e-beam evaporation technique in a BAK 760 e-beam evaporator. The source materials were in a form of 1-3 mm pieces sintered from 99.5% pure ZrC and LaB_6, purchased from CERAC Inc. The e-beam evaporation yielded smooth, uniform, well-adherent deposits on both silicon and oxidized silicon wafers. Table II shows values of growth rate and

resistivity of the films for two cases: substrates not heated during deposition and substrates heated to 250 °C. It can be seen from Table II that resistivities of the evaporated films are only an order of magnitude larger in comparison with the bulk material, and that the resistivity values decrease significantly when the substrate is heated to 250 °C during the deposition. The film resistivity values are comparable to reported resistivities of as-deposited LaB_6 films obtained via DC or RF sputtering from a LaB_6 target.

Table 5. Materials for silicon emitter coatings.

Material	ϕ [eV]	Melting Point [°C]	Resistivity [Ωcm]
LaB_6	1.9-3.4	2530	1.5 x 10-5
ZrC	2.2-3.8	3530	1.7 x 10-4
TaN	1.9	3087	2.0 x 10-4

Table II. Growth rate and resistivity of deposits prepared by e-beam evaporation.

Material	Substrate Temp. [°C]	Growth Rate [nm/min]	Resistivity [Ω cm]
LaB_6	40	60	5.2×10^{-3}
LaB_6	250	50	7.0×10^{-4}
ZrC	40	30	3.0×10^{-3}
ZrC	250	30	8.1×10^{-4}

Chemical composition of the deposited films was analyzed via Auger Electron Spectroscopy (AES), X-ray Photoelectron Spectroscopy (XPS) and X-ray Diffraction Analysis (XRD). The analyses showed that the deposited films are indeed LaB_6 and ZrC. An *ex-situ* XPS analysis of surfaces of the films showed presence of metal oxides. Specifically, the surface of the LaB_6 film was found to contain boron oxides and lanthanum oxides. The molecular ratios of LaB_6 to boron oxides and LaB_6 to lanthanum oxides on the film surface was found to be approximately 2:1 in both cases. Sputtering of the surface was found to result in the removal of the boron oxides and partial removal of the La oxides. The LaB_6 to La oxides ratio in the bulk of the film was determined to be approximately 5:1. In the case of ZrC films, the film surface showed the presence of ZrO_2, with the ZrO_2 to ZrC ratio of about 2:1. The amount of the oxide

decreased rapidly when the surface layer had been sputtered away. It is estimated that the ratio of ZrC to Zr oxides in the bulk of the film is 2:1.

The "bulk" work functions of the deposited films were measured using capacitance vs. voltage (C-V) plots for MOS capacitors prepared with investigated films forming the gate electrode. If two capacitors with two different gate metal electrodes, denoted by *1* and *2*, but with the same oxide layer and the same semiconductor substrate are fabricated, the difference between their flatband voltages is given by (1)

$$V_{FB}^{(2)} - V_{FB}^{(1)} = \varphi_m^{(2)} - \varphi_m^{(1)}. \qquad (1)$$

Work function values for the LaB_6 and ZrC films have been calculated from (1), assuming the work function of 4.2 eV for aluminum. The work function values for the LaB_6 and ZrC films were found equal to 2.2 eV and 2.6 eV, respectively, in agreement with literature values for the bulk materials.

2.3.2 TaN Films. TaN films have been obtained via reactive sputtering of Ta in nitrogen and argon atmosphere, using a Perkin-Elmer 4450 RF sputtering system. The stoichiometric TaN films have been obtained for the following deposition conditions: total system pressure of 6 millitorr, partial pressure of N_2 of 3.5 millitorr and the RF power of 1.56 kW. The resistivity of films deposited in these conditions was $2.2 \times 10^{-4}\ \Omega$ cm, and the film growth rate was approximately 10 nm/min. Chemical composition of the films was verified by the XRD, AES and XPS. As in the case of evaporated films of LaB_6 and ZrC, the surface of TaN films analyzed after the films were exposed to the air contained a small amount of Ta oxide. The ratio of TaN to Ta_2O_5 was found to be equal approximately 3:1 at the surface; the ratio decreased as the bulk of the film was exposed to the analysis. The determination of the work function value for the TaN films is in progress. A dry etching procedure for patterning of TaN films necessary to form MOS capacitors is being developed.

2.3.3 Further Work. The developed techniques will be used to coat gated silicon field emitter arrays, and the influence of the coatings on the emission currents will be assessed. Statistically significant number of field emitter devices with coatings will be electrically tested in the DC and RF modes to evaluate benefits of the coatings for the device performance. Further, we are planning to investigate ways of removing surface contamination (including surface oxides) of the low work function films, since the contamination of the film surface might impede the electron emission.

Integration of the e-beam evaporated LaB_6 and ZrC coatings in the gate device structure is quite straightforward. The films can be deposited on the emitters at the

very end of the device processing sequence. Since the e-beam evaporation of films in the so-called dome configuration is directional, the deposit is formed only on the tip and emitter column, and not on the sidewalls of the inter-electrode insulator (this could cause shorting between the gate metal and the cathode). On the other hand, if TaN is going to be used as the silicon emitter coating, it would have to be deposited at an earlier stage of the device processing sequence, before the formation of the inter-electrode insulator. The issues related to the integration of the TaN coating will be investigated as part of a future work.

In addition, we are considering examining metal silicide coatings and their influence on the emission current characteristics. Some metal silicides (most notably chromium silicides) exhibit lower work functions that silicon, higher melting points and better oxidation resistance. They can be formed via deposition of the metal on the silicon surface and annealing of the structure to a required alloying temperature. Devices coated with chromium (and other) silicides will be tested, and their performance will be compared with that of uncoated devices.

2.4 Vacuum testing and microencapsulation bonding system. One of the projected goals of the ARPA field emitter program at MCNC is the microencapsulation of field emitter devices into triode configuration, wherein the field emitter arrays would have their own vacuum environment and anode electrode built directly into the device structure. Under these circumstances, no external vacuum would need to be provided in order for them to function. As a way of designing such a structure, the engineers at MCNC envisioned a vacuum triode, which would be formed by physically bonding two silicon wafers together face-to-face in vacuum. The field emitter arrays themselves would be present on one wafer; the other wafer would be patterned with a collector metal designed to cap off each array into its own separate vacuum cell. These two wafers would be sealed to one another at high temperatures using an adhesive material to form a vacuum-tight bond. To perform this process, however, a special chamber would be required which could simultaneously provide vacuums as high as 10^{-6} torr, and temperatures as high as 800 °C. At the time of contract award there was no such equipment at MCNC suitable for this type of vacuum bonding.

At the same time, however, there was also a need for a vacuum chamber specifically designed for electrical testing. Having a test-chamber on-site would be advantageous in that the field emitter devices could be tested immediately after fabrication, without the delays and low throughput involved with having the devices tested elsewhere. Initially, it was planned that a vacuum chamber be built primarily for purposes of wafer bonding that could serve equally well for general testing. It was with

these considerations that money was set aside in the ARPA program's equipment budget for a system capable of operating in two separate modes: 1) as a vacuum oven, and 2) as a chamber for electrical testing.

During the initial period of engineering for the system, however, it became obvious that having two separate vacuum chambers would be more advantageous than a single chamber capable of performing both necessary functions. With appropriate scheduling, it might then be possible to run a wafer bonding process on one wafer simultaneously with a test process on another, each in its own chamber. Keeping the two processes separated would help preserve the purity of the test environment, since the contamination level in the vacuum oven would likely be quite high. Designating the vacuum oven as "dirty" would also allow the installation of a retractable evaporation coil, enabling the experimental deposition of materials directly onto the field emitter tips prior to bonding.

The system was initially commissioned in mid-December of 1991 with a local company, LitCo Industries of Raleigh, NC. An intensive period of engineering consultation then followed between LitCo and MCNC, lasting approximately six months. The actual construction of the system was performed in late summer of 1992 by Shrader Scientific of Haywood, CA, and delivered to MCNC on 21 October 1992.

2.4.1 General Description of the System. The system itself is a very simple arrangement, consisting of two entirely separate mirror-image vacuum chambers connected only by a single curved manifold (4" in diameter). This manifold tees off to a common high vacuum source, a CTI-Cryogenics Cryo-Torr 8 cryopump, which is ordinarily rated at 1500 l/s pumping speed (air). For roughing, the chambers are individually plumbed through air-actuated poppet valves. Venting capability for each chamber is similarly configured. To aid in vibration isolation, the mechanical pump is kept outside and away from the main body of the system, and stainless steel flexhose is used for the roughing lines.

Both of the chambers are roughly cylindrical in shape, measuring 15" in height and 12" in outer diameter, and each encloses a space of just over 1620 cubic inches. Chamber wall thickness measures 0.12" along the perimeter, while at the top a bumped head configuration proves slightly larger at 0.125". A 10" diameter conflat base flange caps off the bottom. Loading access is provided in both cases by a second 10" diameter conflat flange located at the front, sealed at four points with a bolt-on door and a Viton O-ring.

The chambers can be isolated from one another (and from the cryopump) by a pair of electropneumatic gate valves set at the ends of the high vacuum line. To handle the valving action during pumpdown and venting cycles, an automatic valve

controller has been installed as part of the system to provide the appropriate crossover sequencing. The controller also acts to protect the integrity of the cryopump by automatically valving it off in the event of an unexpected breach in the system vacuum.

Chamber pressure is monitored over 10 orders of magnitude by means of paired gauges mounted in small side ports on both chambers. A convectron gauge operates from atmosphere down to 10^{-4} torr, while an ion gauge is used at high vacuum (down to 10^{-8} torr). Information from the gauges is routed to a digital display on a pressure gauge controller, where it can be used in activating any of six variable setpoint relays designated for process control.

2.4.2 The Bonding Chamber. The wafer bonding chamber, or vacuum oven, is located on the left side of the system and possesses only five conflat ports equally spaced about its middle, in contrast to the seven on the testing chamber. Four of these are 2.75" in diameter, while the fifth, located directly opposite from the chamber door, has a slightly larger diameter of 3.375".

Two of these five ports are dedicated towards specific uses. The port on the far right is occupied by a small 1.50" diameter window, through which the inner mechanisms can be observed while the chamber is under vacuum. The odd-sized port in the rear is connected to a sealed bellows arrangement which houses an insertion/retraction assembly for the evaporation coil.

The principle occupant of the bonding chamber is a 6" diameter stainless steel wafer press table, which is mounted press table mounted through a long, bellows-sealed shaft to a small exterior air cylinder attached directly beneath the base flange. In the center of the press table is a 4" heating coil under a quartz diffuser. The original design goal was a device capable of supplying sufficient heat and pressure to facilitate the bonding of any wafer pairs loaded within the chamber. During qualification runs, however, it was discovered that the heated stage could not reach the temperature specified in the design. The contractor made a good faith effort to re-fit the heating circuitry, but the design goals could not practically be met. The effort was discontinued when the microencapsulation effort was postponed.

2.4.3 The Testing Chamber. Located on the right side of the system, the testing chamber has seven 2.75" conflat ports ringing its circumference at a height of ten inches from the base. Two have been fitted with 50 Ω SMA electrical feedthroughs rated to 700 V at 1 A for high frequency testing up to 10 GHz. Another port has four MHV connectors rated to 5 kV at 1 A for DC signals. An additional port has four BNC connectors rated to 500 V at 1 A. These connectors are not constant impedance, and so can only be used at DC or low frequencies. One port is dedicated to a UHV compatible micromanipulator. This manipulator, coupled with a removable internal

stage, would give the ability to electrically probe a large number devices on an intact wafer with a single vacuum cycle. The remaining two ports are unused.

Currently the testing chamber is completely empty of any sort of permanent fixtures, except for a quartz dish at the base of the chamber to insulate the high voltages applied to the device test fixture from the chamber walls. An 8" conflat top port is also present on the very top of the chamber with a 6" quartz window viewport there to provide direct examination of the sample being tested.

With the automatic valve controller regulating the pumpdown cycle, the testing chamber pressure falls from atmosphere to the 10^{-7} torr range within an hour. To provide a bakeout stage to the cycle and gain an even better vacuum, two lengths of heating tape have been secured about the girth of the test chamber, directly above and beneath the ring of ports, and an additional heater is affixed to the chamber base. The heating tape has been fitted with thermostat elements to keep the tape temperature constant at 100 °C. Pressures typically in the low 10^{-8} torr can be achieved in the testing chamber with overnight bakeout and pumpdown. This test chamber is in constant use.

3. RECOMMENDATIONS

Phase I of the Field Emitter Array RF Amplifier Development Project has shown that silicon field emitters are viable electron emitting devices. The program performance goals were achieved using devices that are manufacturable using standard IC processing techniques. Large arrays can be fabricated with reasonable yield. Emission currents competitive with metal emitter technology were measured with good repeatability.

Although this project has demonstrated that electron emission can be observed repeatably from silicon field emitter arrays, there is considerable further development required before the technology can be considered mature. Enhancing high frequency performance through further reductions in the device capacitance and increases in the device transconductance is a primary goal. The transconductance can be raised by fine tuning the fabrication process to further reduce the size of the gate aperture diameter. A significant increase in the transconductance can be obtained by incorporating low work function coatings on the emitter tips.

Other areas of research would involve the evaluation of different and better materials for the insulating layer between cathode and the gate electrode. Thermal management of the device must be examined. The theoretical framework also needs to be better understood. While the Fowler-Nordheim relation provides a good first-order approximation of the field emission phenomenon, the effect of work function and geometrical field enhancement on emission in practical devices is still not completely clear. Space charge in the region between the gate and the anode may also play a significant role in the performance of field emission triodes.

If these avenues of research are successfully followed, the silicon field emitter array shows promise as an active element for high frequency amplification. The performance improvements made in this demanding application will have immediate benefit, not only in the RF amplification area, but in less demanding commercial applications as well.

4. FIGURES

Figure 1 Option 1 task schedule in GANTT chart format. Tasks cover the performance period from 4/16/93 through 5/15/94.

Figure 2 Fiscal performance versus projections for basic contract period.

Figure 3 Fiscal performance versus projections for Option 1 contract period.

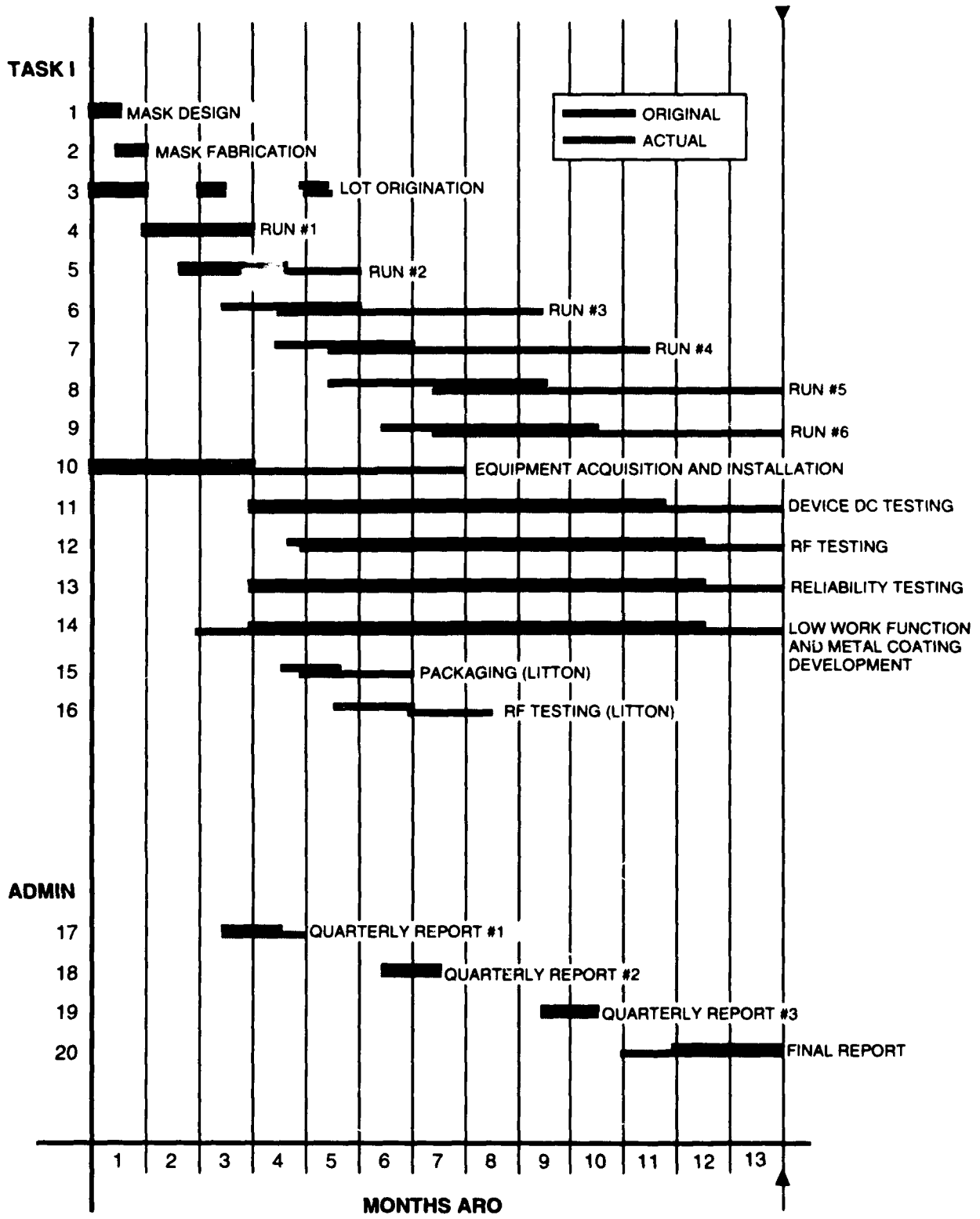
Figure 4 DC emission current collected during RF testing. Plotted as anode current (Ia) versus gate voltage (Vg) to show DC characteristics, and log (Ia/Vg^2) versus 1/Vg to show Fowler-Nordheim behavior.

Figure 5 Oscilloscope screen image displaying the feedthrough signal with the emitter off after calibration, and the output voltage signal (16 mV peak) due to 1 GHz modulation of field emitter array anode current (81 μA peak modulated current).

Figure 6 Free-standing wedge-type column structures produced using crystallographic etching of silicon wafers with a <110> orientation.

Figure 7 Low-capacitance field emitter array with reduced gate electrode metal surface area.

Figure 8 Low-capacitance field emitter array with oxide pillar structure supporting gate metal.



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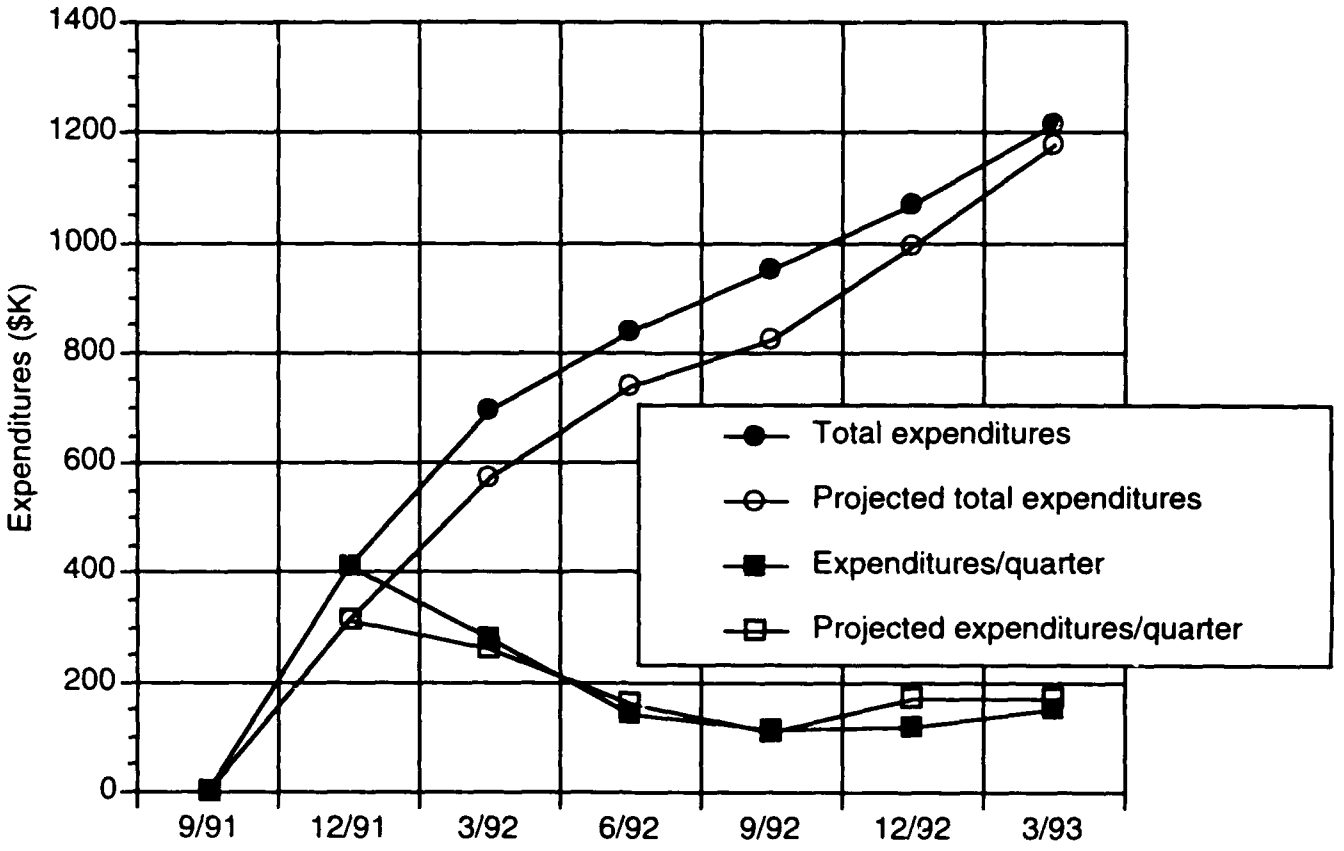


Figure 2
Fiscal performance versus projections for basic contract period.

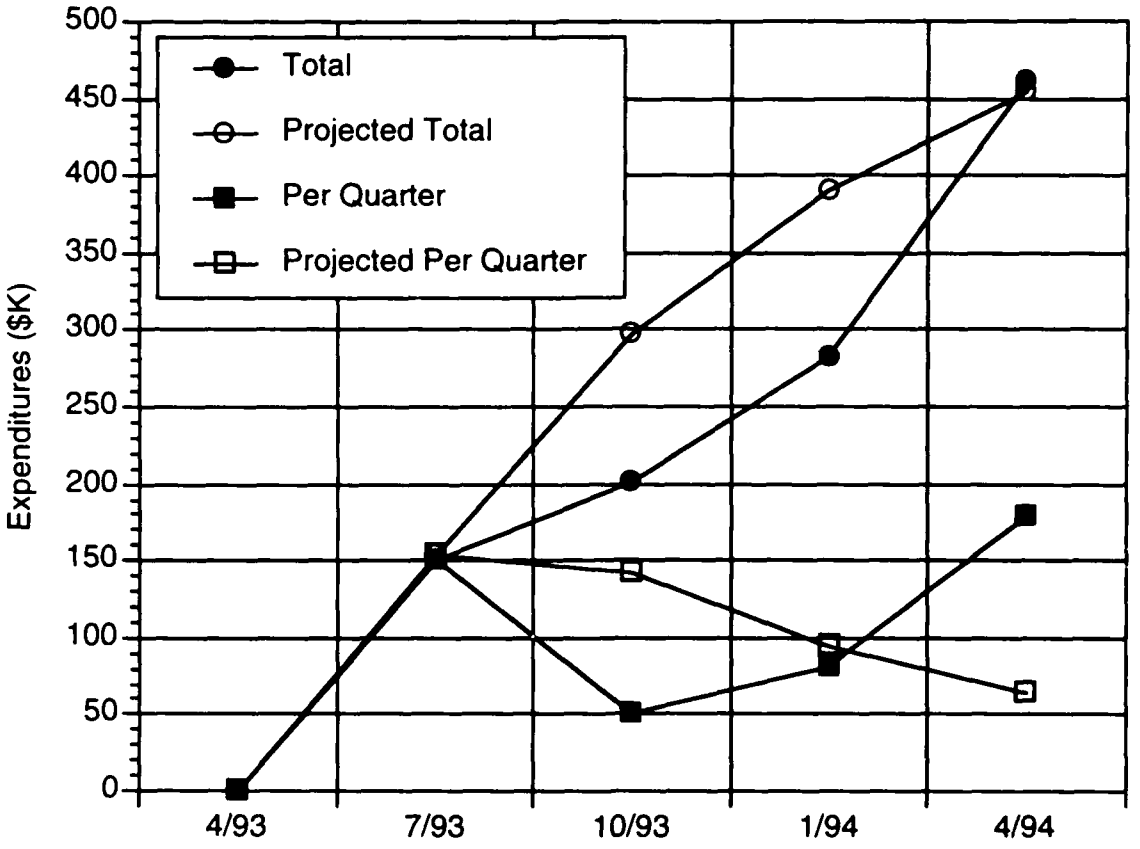
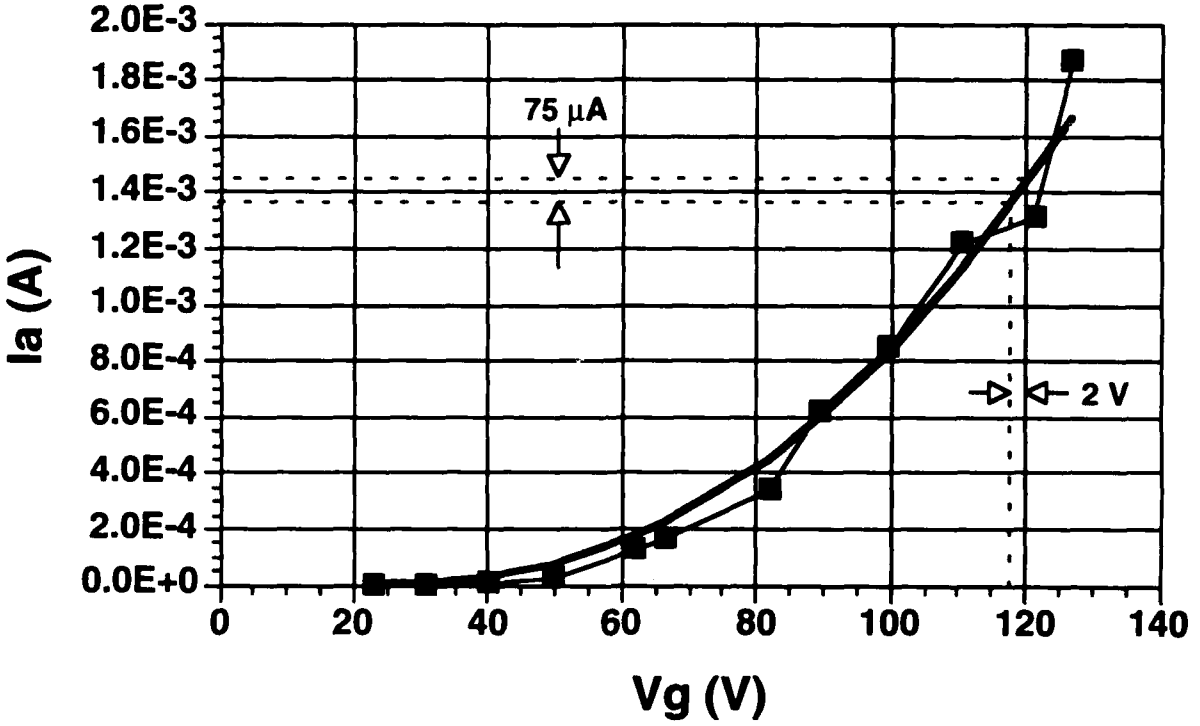
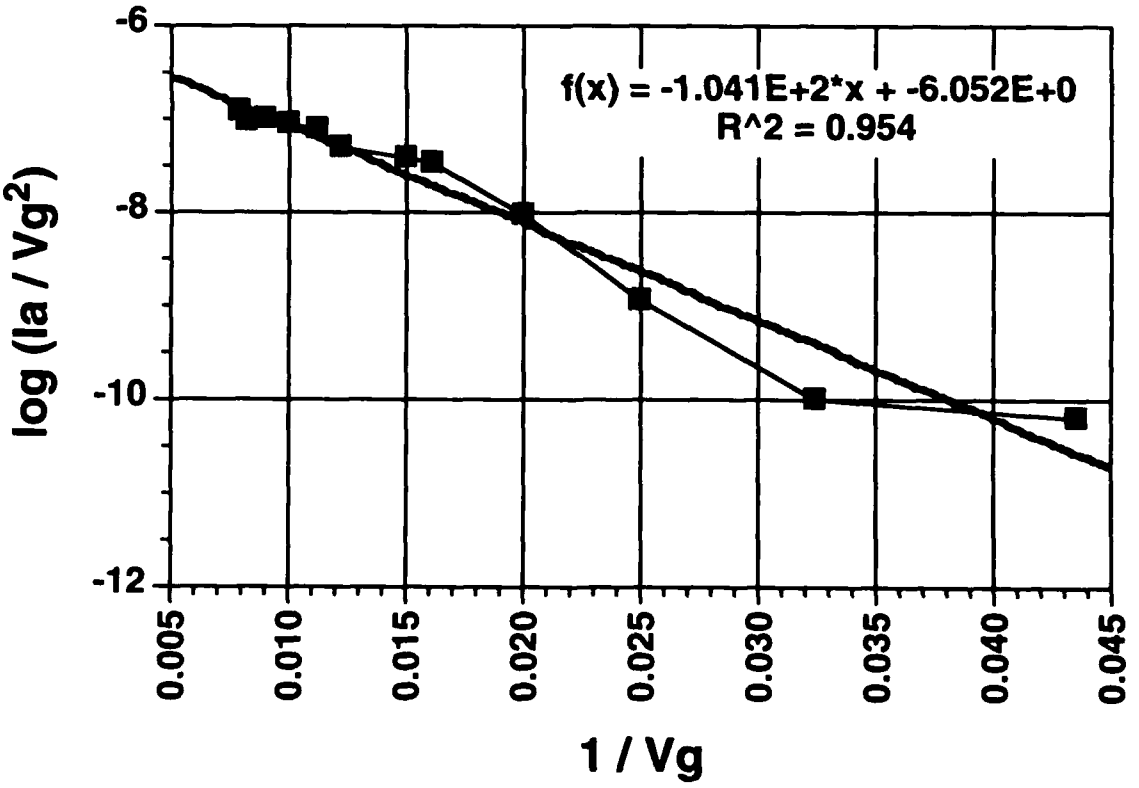


Figure 3
Fiscal performance versus projections for Option 1 contract period.





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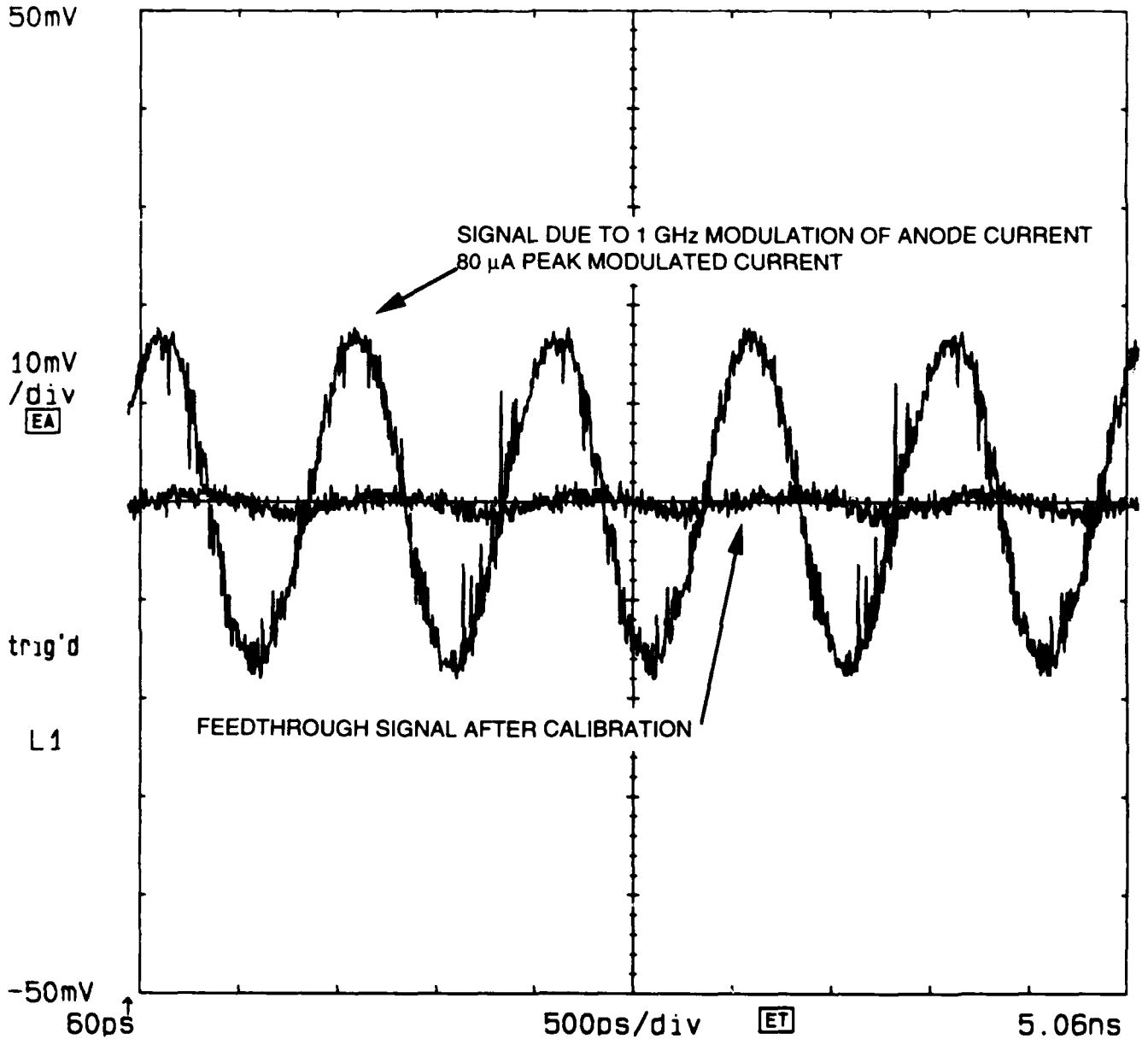

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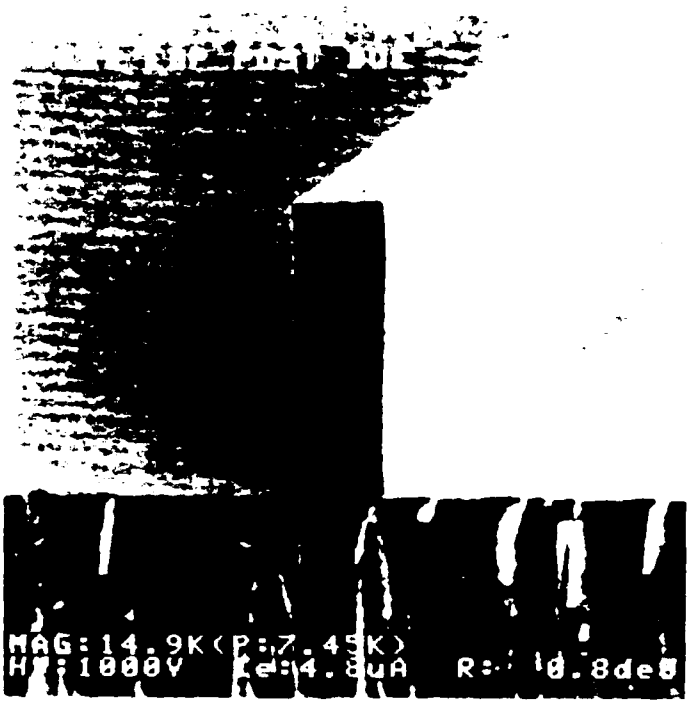

Figure 6
Free-standing wedge-type column structures produced using crystallographic etching of silicon wafers with a <110> orientation.

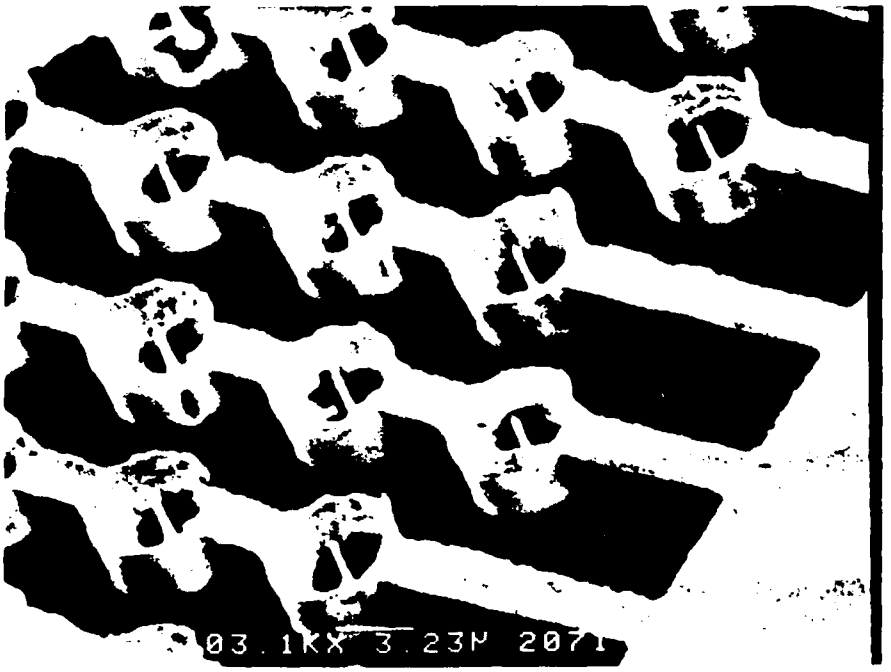

Figure 7
Low-capacitance field emitter array with reduced gate electrode metal surface area.

Figure 8
Low-capacitance field emitter array with oxide pillar structure supporting gate metal.

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APPENDIX A
INDEX OF TECHNICAL REPORTS

The technical reports listed in this appendix are approved for public release with unlimited distribution. The reports are available at the Defense Technical Information Center, Building 5 / Cameron Station, Alexandria, VA 22214.

1. Quarterly Progress Report #1 (9/9/91 – 12/31/91)
2. Quarterly Progress Report #2 (1/1/92 – 3/31/92)
3. Quarterly Progress Report #3 (4/01/92 – 6/30/92)
4. Quarterly Progress Report #4 (7/1/92 – 9/30/92)
5. Quarterly Progress Report #5 (10/1/92 – 12/31/92)
6. Quarterly Progress Report #6 (1/1/93 – 3/31/93)
7. Quarterly R&D Status/Technical Report #7 (4/16/93 – 7/15/93)
8. Quarterly R&D Status/Technical Report #8 (7/16/93 – 10/15/93)
9. Quarterly R&D Status/Technical Report #9 (10/16/93 – 1/15/94)
10. Special Technical Report 11/18/92
11. Special Technical Report 1/17/94
12. Special Technical Report 1/31/94
13. Special Technical Report 2/25/94

APPENDIX B
INDEX OF PUBLICATIONS

B.1 Refereed Journals

1. D. Palmer, J. Mancusi, C. Ball, W. Joines, G. McGuire, D. Temple, D. Vellenga, and L. Yadon. "Measured DC Performance of Large Arrays of Silicon Field Emitters", *IEEE Trans. Elect. Dev.* MS#1050R, in press.

2. D. Temple, C. Ball, D. Palmer, L. Yadon, D. Vellenga, J. Mancusi, and H. Gray. "Fabrication of Column-Based Silicon Field Emitter Arrays for Enhanced Performance and Yield", in preparation.

3. D. Temple, F. Lee, and G. McGuire. "E-Beam Evaporated LaB_6 and ZrC Films for Low Work Function Coatings", in preparation.

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